QPF1003Q

5GHz C-V2X/DSRC/Wi-Fi Front End Module

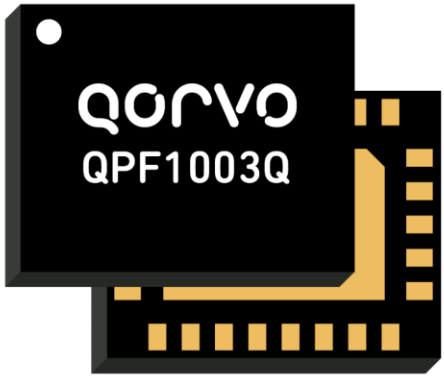
Product Overview

The QPF1003Q is an integrated front end module (FEM) designed for Multi-Standard systems such as C-V2X, DSRC/11p, and Wi-Fi. The compact form factor and integrated matching minimizes layout area in the application.

Performance is focused on optimizing the PA for a 5V supply voltage that conserves power consumption while maintaining the highest linear output power and leading edge throughput.

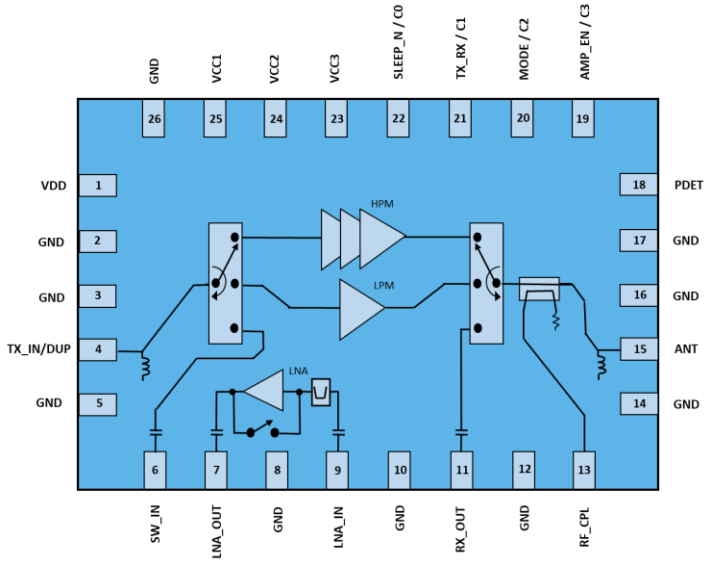
The receive path is pinned out for flexibility to enable external filtering or LNA.

The QPF1003Q integrates a 5 GHz power amplifier (PA), TX/RX Antenna switch and bypassable low noise amplifier (LNA) into a single device



26Pin 5x4x0.925 mm Laminate Package

Functional Block Diagram



Top View

Key Features

- Qualified to AEC-Q100 Grade 2
- Optimized for +5V Operation; +4.2V Capable
- C-V2X Pout = +29 dBm, 10MHz, 12RB
- DSRC/11p Pout = +26 dBm, Class C Mask
- Wi-Fi 11n Pout = +25 dBm, -30 dB EVM
- 27 dB TX Gain
- Tx High Power and Lower Power Modes
- 25 dB TX coupler
- 2.6 dB RX Noise Figure (includes switch)
- 13.7 dB Rx Gain
- 3.6 dB Bypass LNA Loss
- No external matching required

Applications

- ITS C-V2X
- DSRC/11p Applications
- Wi-Fi Infotainment
- Automotive Telematics

Ordering Information

Part Number	Description
QPF1003QSB	5 pc sample bag
QPF1003QSQ	25 pc sample bag
QPF1003QSR	100 pcs on 7” reel
QPF1003QTR13	2500 pcs on 13” reel
QPF1003QEVB	Evaluation board

Absolute Maximum Ratings

Parameter	Conditions	Rating
DC Supply Voltage (V_{CC} & V_{DD})		-0.5 to +5.5V
C3,C2,C1,C0 Control Voltage		-0.5 to V_{DD} + 0.7V
RF Pin 6,7,9,11 DC Voltage	Applicable if external DC voltage is applied to pin	-2.5 to +2.5V
Storage Temperature		-40 to 150 °C
CW RF Input Power at TX_IN	50 Ω Load (No Damage), Transmit Mode	+10 dBm
CW RF Input Power at ANT	(No Damage), Receive LNA On Mode	+15 dBm
CW RF Input Power at ANT	(No Damage), Receive Bypass Mode	+24 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of conditions to the device above the Recommended Operating Conditions up to and equal to the Absolute Maximum Ratings may reduce device reliability.

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Temperature (ambient) [1]	-40		+105	°C
Device Voltage (V_{CC} & V_{DD})[2]	+4.75	+5.0	+5.25	V
C3,C2,C1,C0 Voltage – High	+1.6	+1.8	+3.6	V
C3,C2,C1,C0 Voltage – Low	-0.3		+0.40	V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

[1] Case Temperature allows 10°C max rise over ambient.

[2] Designed to operate down to +4.2V with degraded RF performance with degraded RF performance of 2 dB MPR.

Test Signal Conditions

Name	Definition	MPR
TC1	LTE partial RB: 10MHz, QPSK, RB= 12	0
TC2	LTE full RB: 10MHz, QPSK, RB= 50	1
TC3	LTE 10+10MHz, QPSK, full RB intra-band contiguous CA	2
DSRC/11p	802.11p standard	BPSK, QPSK, 64QAM
Wi-Fi	802.11a/n/ac standard	54Mbps, MCS0, MCS7, MCS9

LTE test signals 3GPP TS25.101 compliant

TX Electrical Specifications (Unless otherwise noted: V_{CC}&V_{DD} =5V, T=+25ºC, LTE Modulation: TC1, QPSK, 10MHz, 12RB, 100% Duty Cycle, MPR=0dB)

C-V2X (TX_IN-ANT) Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Range		5770		5925	MHz
Output Power, HPM	10MHz Modulated, 10% Duty Cycle	-	29	-	dBm
	10MHz Modulated	28	-	-	dBm
	10MHz Modulated (TC2)	27	-	-	dBm
	20MHz Contiguous Intra-Band Modulated (TC3)	26	-	-	dBm
Output Power, LPM	10MHz Modulated	13	14	-	dBm
LTE EVM	Pout ≤ (Pmax), HPM	-	1.67	-	%
	Pout ≤ (Pmax), LPM	-	1.5	-	%
ACPR – EUTRA	(Pout = +0 dBm to Pmax) TC2	-	-43.4	-36	dBc
ACPR – UTRA1	(Pout = +0 dBm to Pmax)	-	-42	-36	dBc
ACPR – UTRA2	(Pout = +0 dBm to Pmax)	-	-57	-37	dBc
Gain	HPM	25	27.15	29	dB
	LPM	7.5	10	12.5	dB
Gain Flatness	In-band across any 10 MHz Channel	-0.15	-	+0.15	dB
Noise Figure, Inband	HPM	-	6	-	dB
	LPM	-	6	-	dB
Out of Band Absolute Gain (HPM)	Cellular Bands 703-2690MHz	-	-8	-	dB
	f = 3300-3800MHz	-	12	-	dB
	f > 7000MHz	-	16	-	dB
TX_IN Port Return Loss	Small signal test (HPM)	-	12	-	dB
ANT Port Return Loss		-	10	-	dB
Quiescent Current, HPM	RF Off	-	287	360	mA
Quiescent Current, LPM		-	89	140	mA
Operating Current, HPM	P_{OUT} = +28 dBm	-	585	720	mA
Operating Current, LPM	P_{OUT} = +13 dBm	-	86.3	150	mA
Efficiency	P_{OUT} = +28 dBm linear power	-	21	-	%
2nd Harmonics	P_{OUT} = +28 dBm, 10MHz (HPM)	-	-17.5	-11	dBm/MHz
3rd Harmonics		-	-69	-60.7	dBm/MHz
2nd Harmonics	P_{OUT} = +13 dBm, 10MHz, (LPM)	-	-41	-35.9	dBm/MHz
3rd Harmonics		-	-70.8	-65.7	dBm/MHz
ANT-LNA_OUT Isolation	TX ON: RF Switch leakage + LNA OFF	-	45	-	dB
ANT-RX_OUT Isolation	TX ON: RF Switch leakage	25.5	29	-	dB
PDET (Power Detect Voltage) HPM[3]	RF OFF	-	0.14	-	V
	Pout = +10 dBm	-	0.31	-	
	P_{OUT} = +20 dBm	-	0.67	-	
	P_{OUT} = +28 dBm	-	0.97	-	

[3] Pdet circuit values of 100ohm series, 10Kohms shunt, 10pF shunt (see applications schematic)

Note: Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

TX Electrical Specifications (Unless otherwise noted: V_{CC}&V_{DD} =5V, T=+25ºC)

DSRC/11p (TX_IN-ANT) Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Range		**5855**		**5925**	**MHz**
Output Power, HPM	10MHz BPSK/QPSK, 100% Duty cycle, meeting ClassC mask	25	26	-	dBm
	10MHz 64QM 27Mbps, 50% Duty Cycle, -28dB DEVM				
Output Power, LPM	10MHz BPSK/QPSK, 100% Duty cycle, meeting ClassC mask	8	10	-	dBm
	10MHz 64QM 27Mbps, 50% Duty Cycle, -28dB DEVM				
Wi-Fi (TX_IN-ANT) Parameter	**Conditions: 50% Duty Cycle**	**Min.**	**Typ.**	**Max.**	**Units**
Frequency Range		**5500**		**5835**	**MHz**
Output Power, HPM	11a, 54Mbps, -28dB DEVM	24	26	-	dBm
	11n, MCS7 HT20/HT40, -30dB DEVM	23	25	-	dBm
	11ac,MCS8/MCS9 VHT20/VHT40, -35dB DEVM	19	22	-	dBm
	11ac,MCS9 VHT80, -35dB DEVM	15	19	-	dBm
Output Power, LPM	11a, 54Mbps, -28dB DEVM	9	12	-	dBm
	11n, MCS7 HT20/HT40, -30dB DEVM	9	11.5	-	dBm
	11ac,MCS8/MCS9 VHT20/VHT40, -35dB DEVM	8	10	-	dBm
	11ac,MCS9 VHT80, -35dB DEVM	7	10	-	dBm
Frequency Range		**5150**		**5500**	**MHz**
Output Power, HPM	11a, 54Mbps, -28dB DEVM,	19	23	-	dBm
	11n, MCS7 HT20/HT40, -30dB DEVM	19	21	-	dBm
	11ac,MCS8/MCS9 VHT20/VHT40, -35dB DEVM	11	14	-	dBm
	11ac,MCS9 VHT80, -35dB DEVM	11	13.5	-	dBm
Output Power, LPM	11a, 54Mbps, -28dB DEVM	9	12	-	dBm
	11n, MCS7 HT20/HT40, -30dB DEVM	9	11.5	-	dBm
	11ac,MCS8/MCS9 VHT20/VHT40, -35dB DEVM	8	10	-	dBm
	11ac,MCS9 VHT80, -35dB DEVM	7	10	-	dBm

Note: Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

RX Electrical Specifications (Unless otherwise noted: V_{CC}&V_{DD} =5V, T=+25ºC, Freq=5150-5925MHz)

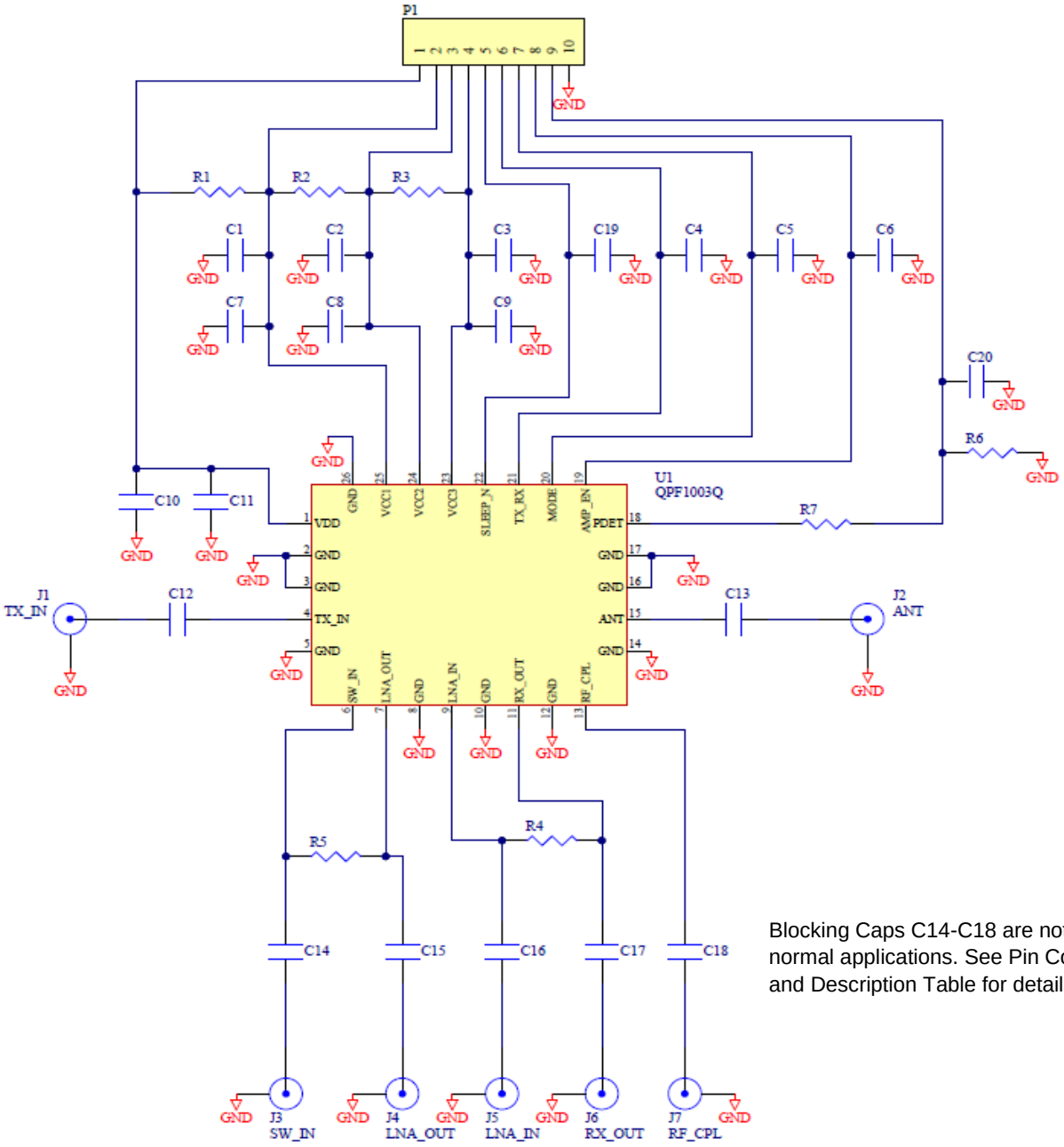
RECEIVE (ANT-RX_OUT)	**Unless otherwise noted: V_{CC}&V_{DD} =5V, T=+25ºC**				
RX Operating Frequency Range		5150	-	5925	MHz
Insertion Loss		-	1.0	1.7	dB
RECEIVE (ANT-LNA_OUT) LNA ON MODE	**Unless otherwise noted: V_{CC}=5V, T=+25ºC Only through path between RX_OUT and LNA_IN**				
Gain		10	13.7	15.7	dB
Gain Flatness	Across any 10 MHz Channel	-0.25		+0.25	dB
Noise Figure		-	2.6	-	dB
LNA_OUT Port Return Loss		-	9	-	dB
ANT Port Return Loss		-	8	-	dB
Out of Band Gain	*Freq* = 2400-2500 MHz	-	-30	-	dB
Input P_{1dB}		-5.1	-1.9	-	dBm
Input IP3		+3.2	+11.7	-	dBm
Rx Operating Current		-	31.5	50	mA
RECEIVE (ANT-LNA_OUT) BYPASS MODE	**Unless otherwise noted: V_{CC}=5V, T=+25ºC Only through path between RX_OUT and LNA_IN**				
Bypass Loss		-7.5	-3.6	-2	dB
Loss Flatness	Across any 10 MHz Channel	-0.20	-	0.20	dB
LNA_OUT Port Return Loss		-	10	-	dB
ANT Port Return Loss		-	10	-	dB
Out of Band Gain	*Freq* = 2400-2500 MHz	-	-30	-	dB
Input IP3		+9	+17.8	-	dBm
Rx Bypass Operating Current		-	2.2	-	mA
RECEIVE (SW_IN-TX_IN/DUP)	**Unless otherwise noted: V_{CC}=5V, T=+25ºC**				
Insertion Loss	Switch ON	-	1.45	2.45	dB
Isolation	Switch OFF	-	10	-	dB
GENERAL SPECIFICATIONS	**Unless otherwise noted: V_{CC}=5V, T=+25ºC, 50 ohm system**				
FEM Leakage Current	Standby Mode	-	25	-	µA
Control Current – High		-	22	-	µA
Control Current – Low		-	<1	-	µA
Coupler	Forward TX Coupling	-26.5	-25	-23.5	dB
	Detected Power Range; +30 to -40 dBm		70		dB
Turn-On Time	50% Vdd to 10/90% RF	-	2	-	µs
Switching Speed, Ramp On/Off	50% Control to 10/90% RF; all states	-	200	-	ns
Junction Temperature[4]	Vcc=5.25V; Pout=29dBm; Tc=105°C		183		°C
Thermal Resistance, θ_{jc}[4]	Junction to case	-	17	-	°C/W
PA Stability – Spurious levels[5]	Output Power Range	0		+30	dBm
	Source/Load, inband, all angles, VSWR ≤ 4:1 at user ANT port	Non-harmonic spurious levels<-41dBm			
Ruggedness[5]	TX_IN +10 dBm; 10:1 mismatch at user ANT port; all phases	No Permanent Damage			

[4] Tj and θ_{jc} based on max operating conditions.

[5] The expected minimum post TX FEM loss = 3dB; typical loss with external filter = 5dB.

Note: Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

Evaluation Board Schematic



Blocking Caps C14-C18 are not needed in normal applications. See Pin Configuration and Description Table for details.

Evaluation Board Bill of Materials

Qty	UOM	Ref Des	Description	Mfg Name	Mfg Part #
1	EA	PCB	PCB, 5.9GHz FEM, Automotive	TTM TECHNOLOGIES INC	QPF1002Q-4000 A
11	EA	C7,C8,C9,C11,C12,C13,C14,C15,C18,C20,R4	CAP, 10pF, 5%, 50V, HI-Q, 0402	MURATA ELECTRONICS SINGAPORE PTE LT	GJM1555C1H100JB01D
1	EA	C10	CAP, 2.2uF, 10%, 10V, X7S, 0.65mm, 0402	TDK SINGAPORE (PTE) LTD	C1005X7S1A225KT000E
4	EA	C4,C5,C6,C19	CAP, 1000pF, 10%, 50V, X7R, 0402	TAIYO YUDEN (SINGAPORE) PTE LTD	UMK105B7102KV-F
1	EA	C3	CAP, 10uF, 20%, 10V, X7T, 0603	MURATA ELECTRONICS SINGAPORE PTE LT	GRM188D71A106MA73D
2	EA	C1,C2	2.2UF,10%,10VDC,X7R,LF,0603,LEAD FREE	MURATA ELECTRONICS SINGAPORE PTE LT	GRM188R71A225KE15D
1	EA	R7	RES, 100 OHM, 1%, 1/10W, 0402	Kamaya, Inc	RMC1/16SK1000FTH
3	EA	R1,R2,R3	RES, 0 OHM, 5%, 1/10W, 0402	Kamaya, Inc	RMC1/16SJPTH
1	EA	R6	RES, 10K, 5%, 1/16W, 0402	Kamaya, Inc	RMC1/16S-103JTH
1	EA	U1	C-V2X/WiFi FEM 5.9GHz		
7	EA	J1,J2,J3,J4,J5,J6,J7	CONNECTOR,SMA EL FLT VIPER MAT-21-1038	AMPHENOL---KAI JACK(SHENZHEN) INC	20-001CH-T
1	EA	P1	CONN, HDR, ST, PLRZD, 10-PIN, 0.100"	AMP	1-640454-0
3	EA	R5,C16,C17	NOT POPULATED ITEM-1		DUMMY PART

Note: A 10pF capacitor was used for R4 when connecting pins RX_OUT to LNA_IN in characterization of this device.

Evaluation Board Information

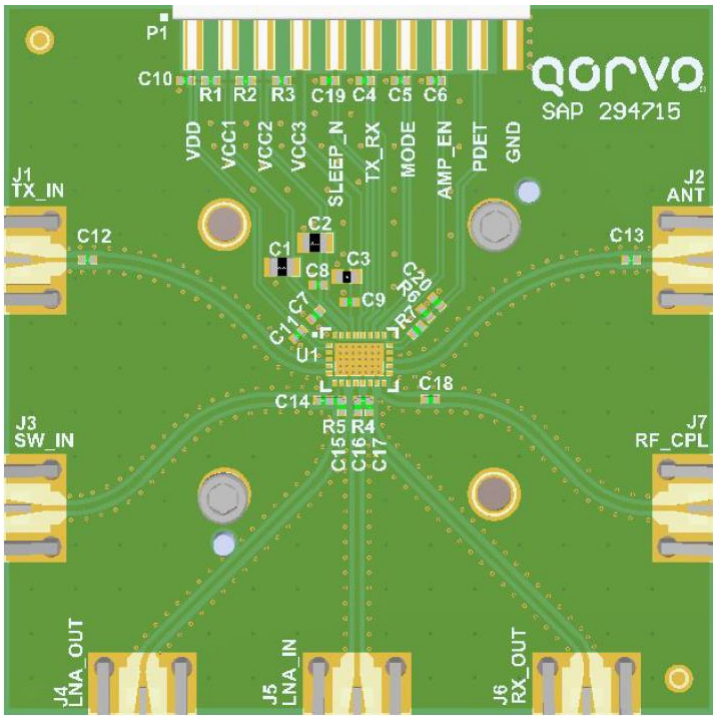
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	0.70mil		
4	Dielectric1	RO4003	8.00mil	3.55	
5	MidLayer1	Copper	0.70mil		
6	Dielectric2	FR4	42.00mil	4.26	
7	MidLayer2	Copper	0.70mil		
8	Dielectric3	RO4003	8.00mil	3.55	
9	Bottom Layer	Copper	0.70mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	

TOTAL THICKNESS: 0.062 +/- 10%

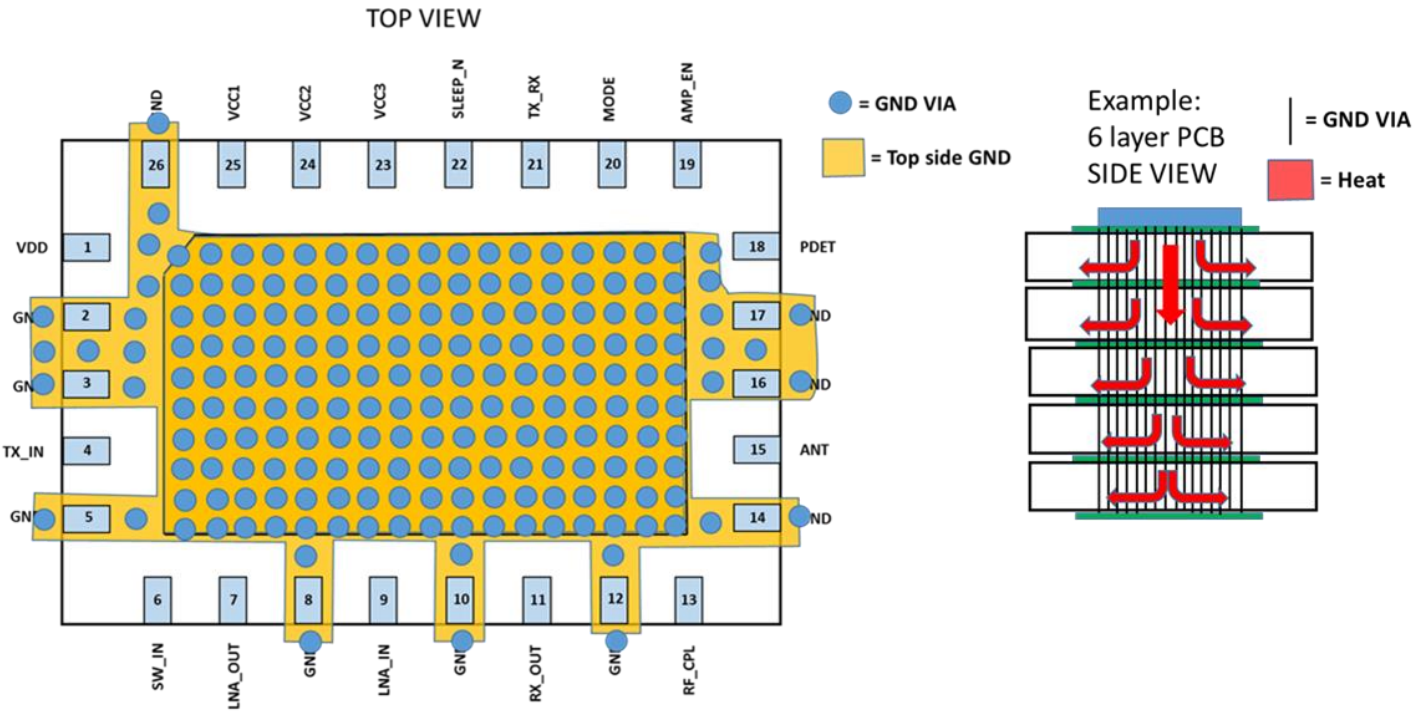
CONTROLLED IMPEDANCE: ☒ YES ☐ NO

CPW LAYER 1:	0.01425+/-0.001	REF LAYER 2
TARGET IMPEDANCE:	50 OHMS +/-5%	
TARGET FREQUENCY:	2.5GHz to 6GHz	
DIELECTRIC CONSTANT:	See stack-up	

Evaluation Board Layout



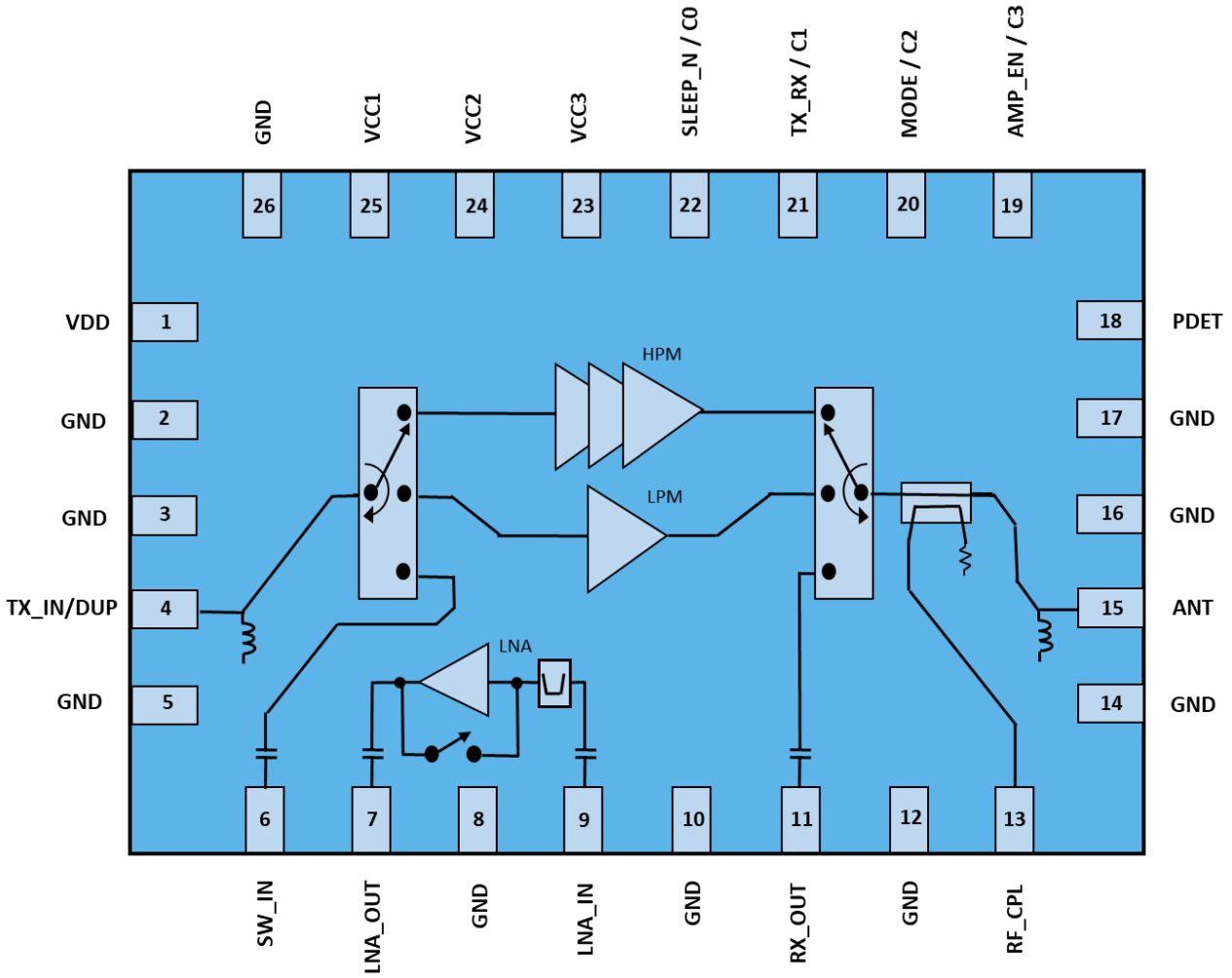
Heat dissipation is a major concern as the device gain is effected by high thermal temperatures. A suggested layout providing a large ground area with adequate GND vias is provided below. Internal ground islands are also suggested to be used to draw heat from the device. The goal is to lower the thermal resistivity to other layers and also lower the electrical inductance.



Pin Configuration and Description

PIN NO.	LABEL	DESCRIPTION
1	V_{DD}	Power Supply pin for RX LNA, RX Bypass, Switches, Logic, LPM PA
2	GND	Ground
3	GND	Ground
4	TX_IN/DUP	TX IN / Duplex Port connected to switch TX port; May also be a duplex common port for TX/RX
5	GND	Ground
6	SW_IN	SW_IN Port connecting to switch RX port. Internally DC blocked.*
7	LNA_OUT	LNA OUT Port connecting to LNA output. Internally DC blocked. *
8	GND	Ground
9	LNA_IN	LNA IN Port connecting to LNA input. Internally DC blocked. *
10	GND	Ground
11	RX_Out	RX Out Port connecting to switch RX port. Internally DC blocked. *
12	GND	Ground
13	RF_CPL	RF Coupler Port connecting to coupled port for forward TX power tap
14	GND	Ground
15	ANT	RF Antenna Port connecting to switch common port
16	GND	Ground
17	GND	Ground
18	PDET	DC power detector. Provides an output voltage proportional to the RF output power level (HPM only)
19	AMP_EN	C3 Logic Control pin, Controls PA and LNA Enable
20	MODE	C2 Logic Control pin, Controls PA and LNA mode select
21	TX_RX	C1 Logic Control pin, Controls internal TX/RX switches
22	SLEEP_N	C0 Logic Control pin, Low state places device in sleep mode
23	V_{CC3}	Power Supply pin for HPM PA final stage
24	V_{CC2}	Power Supply pin for HPM PA second stage
25	V_{CC1}	Power Supply pin for HPM PA first stage
26	GND	Ground

***** Pin DC impedance >250kohm with -2.5V<Vdc<2.5V applied.

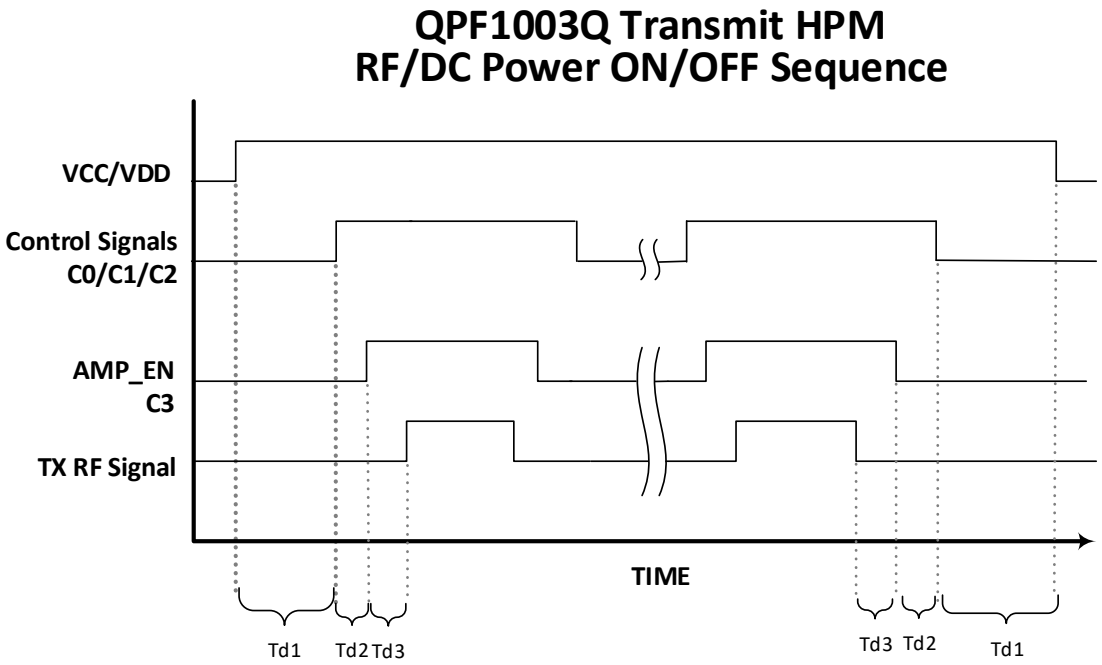


Control – Logic Truth Table

Operation Mode #	Operating Mode	SLEEP_N C0	TX_RX C1	MODE C2	AMP_EN C3	Mode Description
0	Sleep/Standby	Low	X	X	X	All Off
1	TX_HPM_SW	High	High	High	Low	HPM_SW On, All PA Off, LNA Off
2	TX_HPM	High	High	High	High	HPM_PA On, LNA Off
3	TX_LPM_SW	High	High	Low	Low	LPM_SW On, All PA Off, LNA Off
4	TX_LPM	High	High	Low	High	LPM_PA On, LNA Off
5	RX_SW	High	Low	X	Low	RX_SW On, LNA Off, Bypass Off, PA Off
6	RX_LNA	High	Low	High	High	RX_LNA On, All PA Off
7	RX_Bypass	High	Low	Low	High	RX_Bypass On, All PA Off

NOTE: The RF performance is undefined in the Standby state
NOTE: X is a don't care state, either High or Low state

Power On and Off Sequence

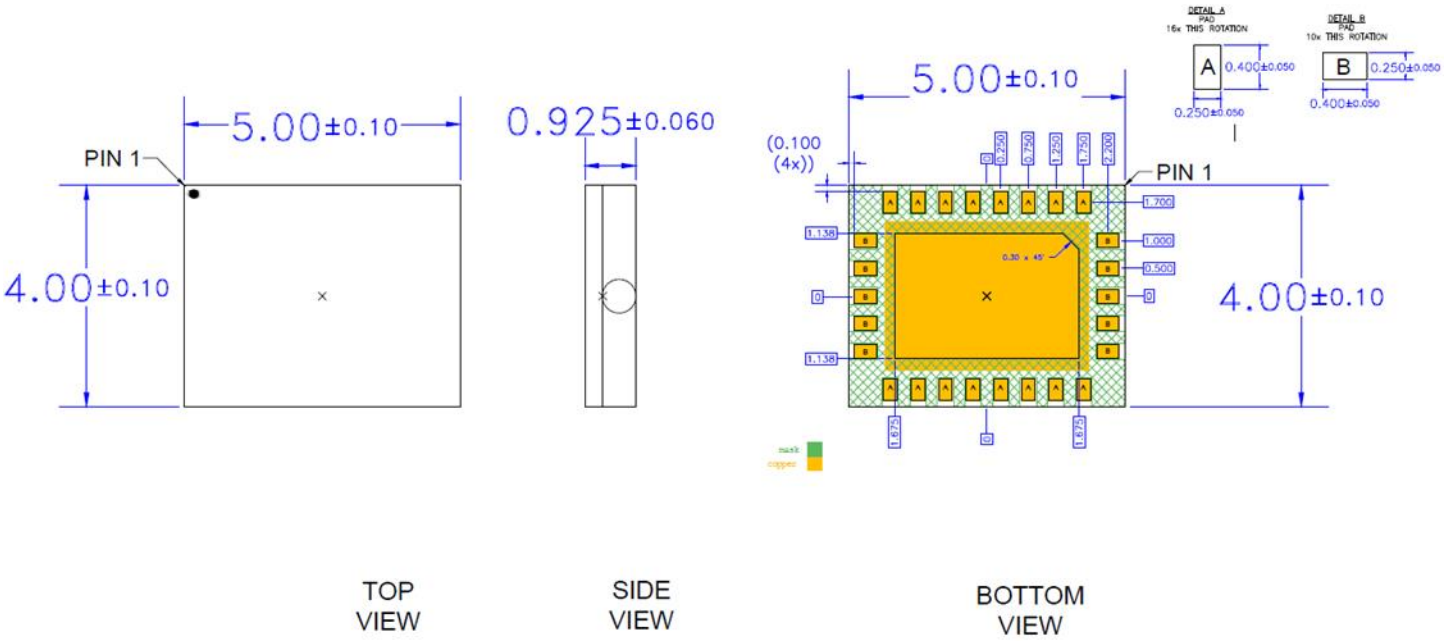


Note:
Observe the timing sequence shown in the diagram above and described below. DC, RF, and Time delay (Td) signal levels per datasheet specificatons.

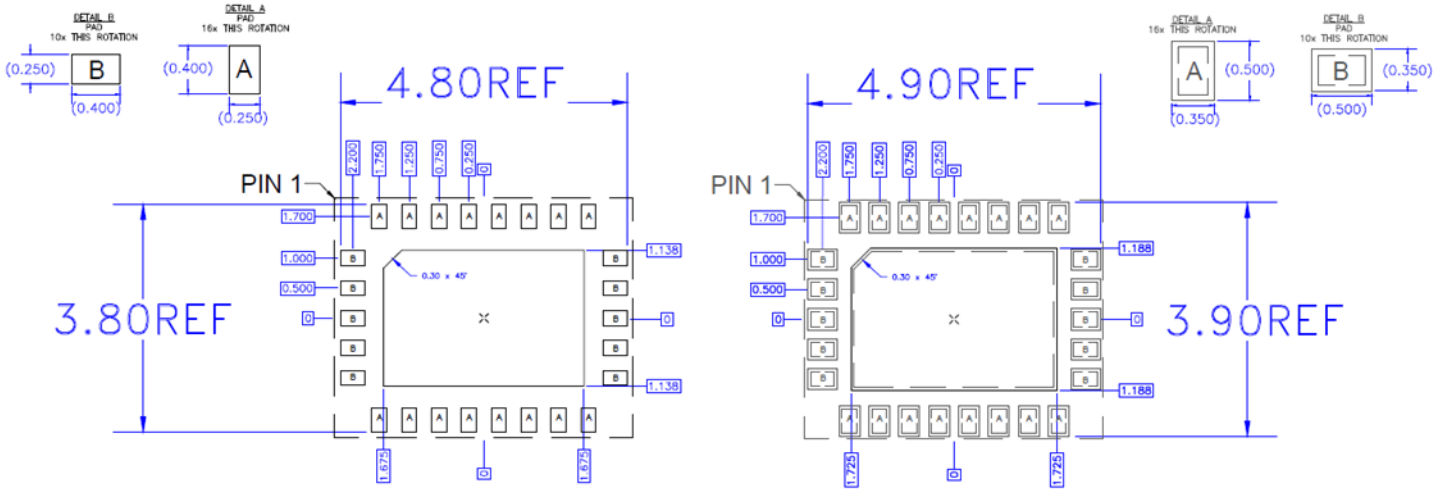
- Apply VCC/VDD prior to turning on or pulsing PA enable
- Turn off PA enable prior to turning off VCC
- Turn on PA enable prior to applying RF signal
- Turn off RF signal prior to turning off PA enable
- Control Signals and AMP_EN may turn HIGH/LOW simultaneously if necessary but recommended to follow Td in diagram
- Td1=5us; Td2=0.2us; Td3=0.5us (no to scale)

Mechanical Information

Package Drawing



PCB Design Requirements



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

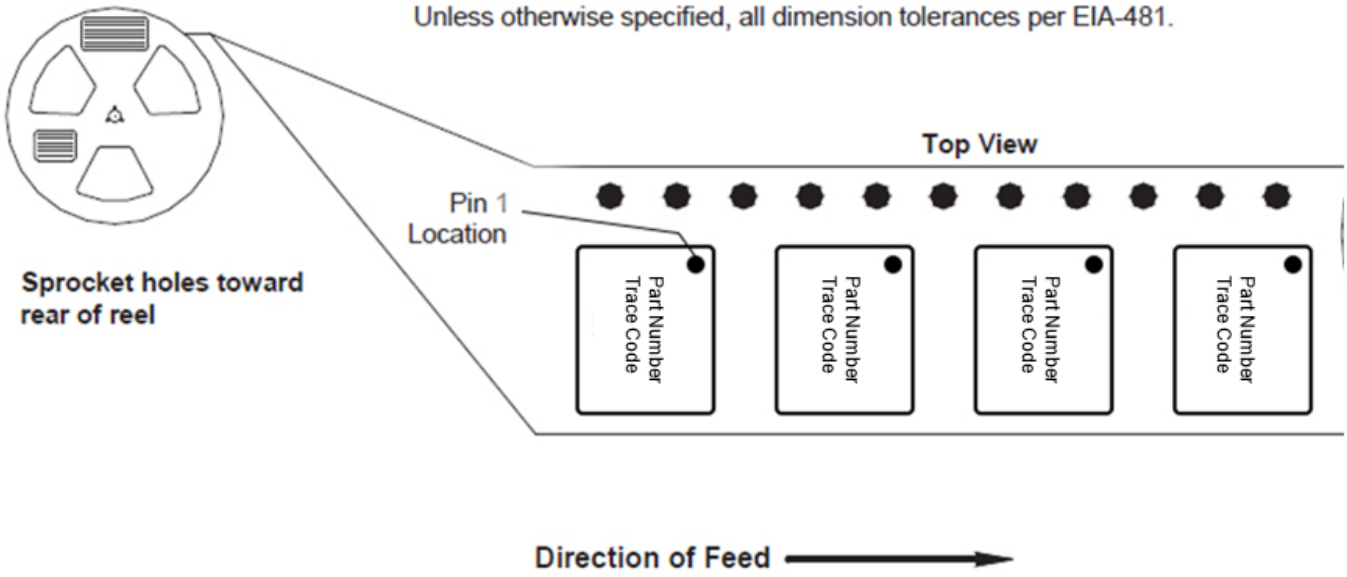
Branding Diagram

Pin 1 Indicator
Qorvo Logo - Use Q5D
Trace Code to be assigned by SubCon

Tape and Reel Information

Table 1. Tape and Reel

Qorvo Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units Per Reel
QPF1003QTR13	13 (330)	4 (102)	12(305)	8(203)	Single	2500
QPF1003QSR	7 (178)	2.5 (63)	12(305)	8(203)	Single	100



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C2a	JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: ENEPIG

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements
Halogen Free (Chlorine, Bromine)
Antimony Free
TBBP-A ($C_{15}H_{12}Br_40_2$) Free
SVHC Free

Revision History

Revision	Description	Date
A	Initial Release	06/07/19
B	Updated specs per final design, updated timing diagram, corrected stability spec, corrected ruggedness spec, corrected Pdet nominal values @ stated power	08/16/19
C	Updated AMR, Specs and Min/Max, EVB Information, Branding diagram, Tape and Reel Information	05/28/20
D	Add Revision History, Updated EVB BOM	05/12/21

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
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